CLAIMS

What is claimed is:

1. A circuit comprising:
   a. a first reference voltage node adapted to provide a first reference voltage;
   b. a reference resistor having:
      i. a first reference-resistor terminal coupled to the first reference voltage node; and
      ii. a second reference-resistor terminal;
   c. a second reference voltage node adapted to provide a second reference voltage;
   d. an on-die termination (ODT) resistor having:
      i. a first ODT-resistor terminal; and
      ii. a second reference-resistor terminal;
   e. a multiplexer having:
      i. a first multiplexer input terminal coupled to the second reference voltage node;
      ii. a second multiplexer input terminal coupled to the second ODT-resistor terminal; and
      iii. a multiplexer output terminal; and
   f. a comparator having:
      i. a first comparator input terminal coupled to the second reference-resistor terminal;
      ii. a second comparator input terminal coupled to the multiplexer output terminal; and
      iii. a comparator output terminal.

2. The circuit of claim 1, further comprising a current source having:
   a. a first current terminal coupled to the second reference-resistor terminal and adapted to receive a first reference current of a first-reference-current magnitude;

b. a second current terminal coupled to the second ODT resistor terminal and adapted to receive a second reference current of a second-reference-current magnitude proportional to the first reference-current magnitude; and

c. at least one current-control terminal adapted to receive a current-control signal;

d. wherein the current source adjusts the first and second magnitudes in response to changes in the current-control signal.

3. The circuit of claim 2, further comprising a feedback loop coupled between the comparator output terminal and the current-control terminal.

4. The circuit of claim 3, wherein the feedback loop includes a current-control register.

5. The circuit of claim 2, further comprising a first load transistor coupled in series with the first current terminal and a second load transistor coupled in series with the second current terminal.

6. The circuit of claim 5, further comprising a current-shorting transistor coupled between the first and second current terminals.

7. The circuit of claim 5, further comprising a second current-shorting transistor coupled between the first and second current terminals via the first and second load transistors.

8. The circuit of claim 7, wherein the first and third reference voltages are substantially equal voltages.

9. The circuit of claim 1, wherein the ODT resistor includes at least one ODT-resistor control terminal, the circuit further comprising a feedback loop coupled between the comparator output terminal and the at least one ODT-resistor control terminal.

10. The circuit of claim 9, wherein the feedback loop includes an ODT-control register.

11. The circuit of claim 1, wherein the comparator alternately compares:
    a. a reference-resistor voltage on the second reference-resistor terminal to the second reference voltage; and
    b. the reference-resistor voltage on the second reference-resistor terminal to an ODT voltage on the second ODT-resistor terminal.

12. The circuit of claim 1, wherein the first and second magnitudes are substantially equal.

13. The circuit of claim 1, wherein the ODT resistor, comparator, and current source are portions of a monolithic integrated device, and wherein the reference resistor is external to the monolithic integrated device.

14. The circuit of claim 1, further comprising a third reference voltage node coupled to the first ODT-resistor terminal.

15. The circuit of claim 1, further comprising:
    a. a plurality of signal nodes receiving input signals;
    b. a plurality of signal-node ODT resistors, at least one ODT termination resistor coupled to each of the signal nodes, each signal-node ODT resistor including a resistor-calibration port; and
    c. an ODT calibration bus coupled between the comparator output terminal and the resistor-calibration ports of the signal-node ODT resistors.

16. The circuit of claim 1, further comprising:
    a. a plurality of signal nodes receiving input signals;
    b. a plurality of signal-node current sources, at least one signal-node current source coupled to each of the signal nodes, each signal-node current source including a current-source calibration port; and
    c. a current-source calibration bus coupled between the comparator output terminal and the current-source calibration ports of the signal-node current sources.

17. A method of calibrating an on-die termination (ODT) resister on an integrated-circuit, the method comprising:
    a. drawing a reference current through a reference resistor having a first reference-resistor terminal, a second reference-resistor terminal, and exhibiting a reference resistance between the first reference-resistor terminal and the second reference-resistor terminal, the reference resistor receiving a first reference voltage on the first reference-resistor terminal and providing a reference-resistor voltage on the second reference-resistor terminal;

b. drawing an ODT current proportional to the reference current through the ODT resister, the ODT resister having a first ODT terminal and a second ODT terminal and exhibiting an ODT resistance, the ODT resistor receiving a second reference voltage on the first ODT-resistor terminal and providing an ODT-resistor voltage on the second ODT-resistor terminal;

c. comparing, with an on-die comparator, the reference-resistor voltage with the ODT resistor voltage to produce a current-correction signal; and

d. adjusting the ODT current in response to the current-correction signal.

18. The method of claim 17, further comprising:

e. comparing, with the on-die comparator, the reference-resistor voltage with the ODT resistor voltage to produce an ODT-resistor-correction signal; and

f. adjusting the ODT resistor in response to the current-correction signal.

19. The method of claim 18, further comprising repeating (a) through (d) of claim 1 to readjust the ODT current.

20. The method of claim 19, further comprising connecting the second reference-resistor terminal and the second ODT-resistor terminal before readjusting the ODT current.

21. The method of claim 18, wherein the ODT current is adjusted before adjusting the ODT resistor.

22. The method of claim 18, wherein the ODT current is adjusted before and after adjusting the ODT resistor.

23. A data communication system comprising:
    a. a first integrated-circuit supporting:
        i. a driver circuit having:
            (1) a driver input node receiving an input data stream;
            (2) a driver output node providing an output data stream derived from the input data stream;
            (3) a driver-current control port receiving a current-control signal;
        ii. a termination element having:
            (1) a termination-element terminal coupled to the driver output node; and
            (2) a ODT-calibration port receiving an ODT-calibration signal; and
        iii. an ODT control system having a resistance-calibration port coupled to the ODT-calibration port, and a current-calibration port coupled to the driver-current control port;
    b. a signal transmission line having a first and second transmission-line nodes, the first transmission-line node coupled to the driver output node; and
    c. a second integrated-circuit supporting a receiver circuit, the receiver circuit having a receiver input node coupled to the second transmission-line node and receiving the output data stream.

24. The system of claim 23, further comprising a reference-voltage source external to the first and second

integrated-circuits and providing a reference voltage to the ODT control system.

25. The system of claim 23, further comprising a reference resistor external to the first and second integrated-circuits and providing a reference resistance, the reference resistor coupled between a reference voltage node and the ODT control system.

26. A digitally controlled termination element extending between a reference-voltage node and a signal transmission line, the termination element comprising:
    a. an N-line ODT control bus receiving an N-bit ODT offset count;
    b. a first binary-weighted resistive portion having a plurality of parallel resistive paths extending between the reference-voltage node and the signal transmission line, each resistive path including a transistor coupled in series with at least one resistor and having a control terminal coupled to one of the N lines of the ODT control bus; and
    c. a second resistive portion coupled in parallel with the first resistive portion between the reference-voltage node and the transmission line, wherein the second resistive portion exhibits at least three levels of series resistance.

27. The termination element of claim 26, wherein the second resistive portion includes a second transistor coupled between the reference-voltage node and the transmission line, the second transistor having a control terminal coupled to another of the N lines of the ODT control bus.

28. The termination element of claim 26, wherein the second resistive portion includes a voltage divider, the voltage divider having a plurality of voltage-divider resistors coupled in series between the reference-voltage node an the transmission line.

29. The termination element of claim 28, wherein the voltage divider further comprises a plurality of voltage-divider transistors, each voltage-divider transistor coupled in parallel with a respective one of the voltage-divider resistors.

30. The termination element of claim 29, wherein each voltage-divider transistor includes a control terminal coupled to one of the N lines of the ODT control port.

31. The termination element of claim 26, wherein the second portion includes an integrator.

32. The termination element of claim 31, wherein the second portion includes a second transistor coupled between the reference-voltage node and the transmission line and having a second control terminal coupled to the integrator.